A M E N D M E N T

IN THE CLAIMS:

Please **AMEND** claims 1, 4, 16, and 19, **CANCEL** claims 2, 5 to 14, and 20 to 26, and **ADD** claim 27 such that the claims read as follows:

1. (Currently Amended) A method for controlling the flow of data between a first and second clock domain comprising:

selecting one of a plurality of ports included in a physical layer interface in the second clock domain to which to send data; and

transmitting data from a transmit buffer in the first clock domain to the selected port in the physical layer interface in the second clock domain,

wherein selecting one of the plurality of ports included in the physical layer interface in the second clock domain to which to send data includes:

polling each of the plurality of ports in the physical layer interface in the second clock domain to determine polling results indicating available ports which may receive data;

sending the polling results to the first clock domain; and

selecting, in the first clock domain, a port from the available ports included in the physical layer interface in the second clock domain to which to send data, and

wherein sending the polling results to the first clock domain includes sending the polling results to the first clock domain after a predetermined portion of a previous data

transmission from the transmit buffer in the first clock domain to the selected port in the physical layer interface in the second clock domain is complete.

2. (Cancelled)

3. (Original) The method of claim 1 wherein transmitting data from the transmit buffer in the first clock domain to the selected port in the physical layer interface in the second clock domain includes:

transmitting data for the selected port from the transmit buffer to an asynchronous buffer;

transmitting the data from the asynchronous buffer to an internal buffer of a physical layer device included in the physical layer interface, the physical layer device including the selected port; and

transmitting the data from the internal buffer of the physical layer device to the selected port.

4. (Currently Amended) The method of claim 3 further comprising resetting the polling results after a predetermined portion of a data transmission from the asynchronous buffer to the selected port in the physical layer interface in the second clock domain is complete.

5. to 14. (Cancelled)

15. (Original) A network processor comprising:

a transmit buffer in a first clock domain;

a first asynchronous buffer coupled to the transmit buffer;

a first physical layer interface, in a second domain, coupled to the first asynchronous buffer, the first physical layer interface including a plurality of physical layer devices;

a second asynchronous buffer coupled to the transmit buffer;

a second physical layer interface, in a third clock domain, coupled to the second asynchronous buffer, the second physical layer interface including a plurality of physical layer devices; and

logic adapted to:

select one of a plurality of ports included in one of the first and second physical layer interfaces to which to send data; and

transmit data from the transmit buffer to the selected port.

16. (Currently Amended) An apparatus comprising:

a transmit buffer in a first clock domain;

an asynchronous buffer coupled to the transmit buffer;

a physical layer interface, in a second domain, coupled to the asynchronous buffer, the physical layer interface including a plurality of physical layer devices each having a plurality of ports;

control logic coupled to the asynchronous buffer and the physical layer interface, and adapted to:

poll each of the plurality of ports in the physical layer interface in the second clock domain to determine available ports which may receive data;

send polling results to the first clock domain; and

select logic coupled to the transmit buffer and asynchronous buffer, and adapted to:

select, in the first clock domain, a port from the available ports included in the physical layer interface in the second clock domain to which to send data; and

transmit data from the transmit buffer in the first clock domain to the selected port in the physical layer interface in the second clock domain,

wherein the control logic is further adapted to send the polling results to the first clock domain after a predetermined portion of a previous data transmission from the transmit buffer to the selected port in the physical layer interface is completed.

17. (Cancelled)

18. (Original) The apparatus of claim 16 wherein the select logic is further adapted to:

transmit data for the selected port from the transmit buffer to the asynchronous buffer;

transmit the data from the asynchronous buffer to an internal buffer of a physical layer device included in the physical layer interface, the physical layer device including the selected port; and

transmit the data from the internal buffer of the physical layer device to the selected port.

19. (Currently Amended) The apparatus of claim 18 wherein the control logic is further adapted to reset the

polling results after a predetermined portion of ~~a~~ the data transmission from the asynchronous buffer to the selected port in the physical layer interface is completed.

20. to 26. (Cancelled)

27. (New) An apparatus comprising:

a transmit buffer in a first clock domain;

an asynchronous buffer coupled to the transmit buffer;

a physical layer interface, in a second domain, coupled to the asynchronous buffer, the physical layer interface including a plurality of physical layer devices each having a plurality of ports;

control logic coupled to the asynchronous buffer and the physical layer interface, and adapted to:

poll each of the plurality of ports in the physical layer interface in the second clock domain to determine available ports which may receive data;

send polling results to the first clock domain; and

select logic coupled to the transmit buffer and asynchronous buffer, and adapted to:

select, in the first clock domain, a port from the available ports included in the physical layer interface in the second clock domain to which to send data; and

transmit data from the transmit buffer in the first clock domain to the selected port in the physical layer interface in the second clock domain,

wherein the select logic is further adapted to:

transmit data for the selected port from the transmit buffer to the asynchronous buffer;

transmit the data from the asynchronous buffer to an internal buffer of a physical layer device included in the physical layer interface, the physical layer device including the selected port; and

transmit the data from the internal buffer of the physical layer device to the selected port,

wherein the control logic is further adapted to reset polling results after a predetermined portion of a data transmission from the asynchronous buffer to the selected port in the physical layer interface is completed.